

(SYLLABUS)

1.

(Course Title)		(Instructor)			
(Year)	2025	(Semester)	1	(Course No.)	2150078601
(Class)	01	(Open to)	2, 3, 4	(Course Classification)	-
/	3.0 / 03 / 3		100	가	가
(Office)		(Telephone)	02-820-0976	(e-mail)	roger@ssu.ac.kr
	(PBL), (TBL)		+		2023
	(*) (ABEEK Classification)		(*) (ABEEK Requirement)		
(Course Description)	. HDL				

Verilog-HDL      Simulation/Synthesis      FPGA	

가	( 100 )	( 100%)
	50	50
	25	25
	15	15
	10	10

## (SYLLABUS)

(Required Texts)		
	( )	* /Digital Design/F. Vahid/Wiley/2011/2nd ed. * / / : L. / /2016/2 * /Digital Design/ /2023
	AMD Xilinx S/W Vivado PC Vivado가 PC Vivado . . Vivado S/W ppt SW가 PC (Vivado install.ppt).	
	[ - Engaged Learning + - ( ) - FPGA FPGA , Vivado Simulation	
Vivado Install.pptx		

2.

(Week)	(Keyword)	(Description)		(Texts)
01	,	/ /	, , , ,	
02	,	/ ( )	, , , ,	
03		2 K-Map 2	, , , ,	
04	1	; /	, , , ,	
05	2	; /	, , , ,	
06	Testbench,	Schematic/Verilog HDL Testbench	, , , ,	
07		Full Adder	, , , ,	
08	,	1 , SR latch , JK-, D- Flip-Flop	, , , ,	
09		Clocks ,	, , , ,	
10	Finite State Machines 1	FSM(Finite State Machine) , FSM	, , , ,	
11	Finite State Machines 2	FSM ,	, , , ,	
12	Counter	Decimal Counter	, , , ,	

(SYLLABUS)

13		Multi-function Counter	, , , ,	
14		( )	, ,	
15			, , , , ,	

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(SYLLABUS)

3. ( )

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	Open-ended problem		
	Teamwork		
	Communication skills		